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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,826	08/18/2003	Marco Wirasinghe	42P15529	7008

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	PAPER NUMBER
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/643,826	WIRASINGHE ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 4, 2006 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicholson et al. (PGPUB: US 2004/0153694) in view of Lee et al. (USPN: 5,809,223).

Regarding claims 1-2, Nicholson discloses requesting an operating system to place a computer system in a hibernation mode (refer to Figure 7, the system determines whether it is entering hibernation, this determination is intrinsically in response to a stimuli of some sort requesting that the system enters hibernation, furthermore, since the operating system controls the allocation and usage of hardware resources, it is evident that the operating system receives such stimuli/request); gathering a state of the computer system (Figure 7, Reference 710); storing the system state to a first non-volatile memory of the computer system (Figure 7, Reference 712), and storing the system state to a second non-volatile memory of the computer system (Figure 7,

Reference 714). Nicholson does not explicitly disclose the second non-volatile memory internal to the computer system. However, Lee teaches the concept of storing the state of the computer system to a first and second memory internal to the computer system when the system is placed in hibernation mode (C 7, L 48-53). This feature provides improved performance by storing the data locally, which reduces delays associated with non-local data transfers. Hence, one of ordinary skill in the art would have been motivated to modify Nicholson's teachings to provide the second memory internal to the computer system for the desirable purpose of improved performance.

Regarding claim 3, Nicholson discloses the first non-volatile memory has a storage capacity between 50-2000 megabytes (section [0042]), wherein the second non-volatile memory has a greater storage capacity than the first non-volatile memory (section [0004]; the remote boot server contains a hard disk drive and the smallest size of such a drive is 30 GB).

Regarding claim 4, the first non-volatile memory is logically coupled to the second non-volatile memory (section [0038], 2nd column, lines 9+, the second non-volatile memory is coupled to the first via References 171, 170, 121, and 222 in Figure 1).

Regarding claim 5, Nicholson and Lee disclose powering off the computer including powering off the second non-volatile memory (Figure 7, Reference 708; pursuant to the modification of the system where the second memory is internal to the computer system, the computer system and all of its elements are powered off when the computer system is powered off).

Regarding claim 6, Nicholson discloses powering on the computer system (section [0055], lines 16+); and loading the system state from the first non-volatile memory (Figure 9, step 806).

Regarding claim 7, Nicholson discloses the system state comprising contents of central processing unit (section [0052], lines 1-6; the system saves all information required to restore the system, since the central processing unit performs all of the processing for the system [section [0039], it is evident that the state of the cpu or contents of the cpu are required for storage when the system hibernates in order to ensure that the processing unit may resume processing).

Regarding claim 8, Nicholson discloses requesting that a computer system be placed in a hibernation mode (refer to Figure 7, the system determines whether it is entering hibernation, this determination is intrinsically in response to a stimuli of some sort requesting that the system enters hibernation); writing a state of the system to a hard disk drive of the computer system having a non-volatile memory cache (section [0010; lines 6+; the remote boot server comprises a hard disk drive comprising a non-volatile memory cache); storing the state of the system to the hard disk drive cache (section [0011]); reducing power to the computer system (Figure 7, Reference 708). The hard disk drive, which stores the system state during hibernation mode, is remote and thus is not necessarily powered off when the computer system is powered off. However, Lee teaches the concept of providing a memory in the computer system to store the system state (C 7, L 48-53). This feature provides improved performance by storing the data locally, which reduces delays associated with non-local data transfers. Hence, one of ordinary

skill in the art would have been motivated to modify Nicholson's teachings to provide the second memory internal to the computer system for the desirable purpose of improved performance. Pursuant to the modification of the system where the second memory is internal to the computer system, the computer system and all of its elements are powered off when the computer system is powered off, including the hard disk drive).

Regarding claim 9, Nicholson discloses requesting data from the cache to restore the state of the system after hibernation (section [0010], lines 12+).

Regarding claim 10, Nicholson discloses a mobile computer system (section [0028]; a mobile computer system is a computer system used in a mobile environment).

Regarding claim 11, Nicholson discloses a desktop computer system (section [0028 and 0050]; Nicholson discloses a computer system using a Windows operating system; such a system is a desktop computer system).

Regarding claims 12, 19 and 30, Nicholson discloses requesting that a computer system having a hard disk drive (section 0038, lines 17-20]) and a non-volatile memory (Figure 1, Reference 208) coupled to (via References 170, 171, 121 and 222 in Figure 1) a hard disk drive (Figure 1, Reference 183; the remote boot server contains a hard disk drive) of a mobile or desktop computer (section 0028, lines 10+; section 0030) be placed in hibernation mode (refer to Figure 7, the system determines whether it is entering hibernation, this determination is intrinsically in

response to a stimuli of some sort requesting that the system enters hibernation); determining an address location of the non-volatile memory and writing contents of a central processing unit to the non-volatile memory (section [0052], lines 1-6; the system saves all information required to restore the system, since the central processing unit performs all of the processing for the system [section [0039], it is evident that the state of the cpu or contents of the cpu are required for storage when the system hibernates in order to ensure that the processing unit may resume processing; reducing power to the computer system (Figure 7, Reference 708). The hard disk drive, which stores the system state during hibernation mode is remote and thus is not necessarily powered off when the computer system is powered off. However, Lee teaches the concept of providing a memory in the computer system to store the system state (C 7, L 48-53). This feature provides improved performance by storing the data locally, which reduces delays associated with non-local data transfers. Hence, one of ordinary skill in the art would have been motivated to modify Nicholson's teachings to provide the second memory internal to the computer system for the desirable purpose of improved performance. Pursuant to the modification of the system where the second memory is internal to the computer system, the computer system and all of its elements are powered off when the computer system is powered off, including the hard disk drive). Additionally, since the non-volatile memory is a separate native device, [refer to section [0041, lines 19+], it is evident that the address of such a device must be determined before data is stored thereto). Nicholson discloses performing the above features by a personal computer/CPU executing computer readable instructions [section [0028]).

Additionally, regarding claim 30, Nicholson does not disclose the first non-volatile memory having the same address configuration as the second non-volatile memory (hard disk drive). This concept is well known with cache memory and main memory applications, wherein the cache and main memory having a same address configuration. This feature allows data to written to the cache and the main memory during a write through process, which ensures that the main memory will always be synchronized with the cache in the event of failures. Nicholson discloses the use of the first and second memory to improve reliability in the event of errors or failures and thus it would have been obvious to one of ordinary skill in the art to incorporate this well known concept in the system taught by Nicholson for the desirable purpose of improved reliability.

Regarding claim 13, Nicholson discloses writing contents of an operating system to the non-volatile memory (section [0050]).

Regarding claims 14 and 30, Nicholson discloses writing contents of a random access memory to the non-volatile memory (section [0052], lines 1-12; the RAM stores data/programs presently operated on and thus this information would be used prior to hibernation and thus would be stored in the non-volatile memory, also refer to section [0028]).

Regarding claim 15, Nicholson discloses powering off the computer (Figure 7, step 708).

Regarding claims 16-18 and 32-33, Nicholson discloses awakening the computer system from the hibernation mode and initiating a load sequence from the non-volatile memory to restore the system to the contents of the central processing unit (Figure 9, step 806 and step performed before 806; also refer to section [0028]).

Regarding claims 20-21, Nicholson discloses a central processing unit (CPU) (Figure 1, Reference 120); a main memory coupled to the CPU, wherein the memory stores data to be manipulated by the CPU (Figure, Reference 130); a first non-volatile memory coupled to the main memory, wherein the data of the main memory is stored to the first non-volatile memory if the system is placed in hibernation mode (Figure 1, Reference 208; Figure 7, References 710 and 712); and a second non-volatile memory (Figure 1, Reference 182; the remote boot server comprises a hard disk drive which is larger that the first the non-volatile memory) coupled to the first non-volatile memory, wherein the second non-volatile memory has a greater storage capacity that the first non-volatile memory (section [0042]), (section [0004]; the remote boot server contains a hard disk drive and the smallest size of such a drive is 30 GB). Nicholson does not disclose the first non-volatile memory having the same address configuration as the second non-volatile memory. This concept is well known with cache memory and main memory applications, wherein the cache and main memory having a same address configuration. This feature allows data to written to the cache and the main memory during a write through process, which ensures that the main memory will always be synchronized with the cache in the event of failures. Nicholson discloses the use of the first and second memory to improve reliability in the event of errors or failures and thus it would have been obvious to one of ordinary skill in the art

to incorporate this well known concept in the system taught by Nicholson for the desirable purpose of improved reliability. Additionally, Nicholson does not explicitly disclose the second non-volatile memory internal to the computer system. However, Lee teaches the concept of storing the state of the computer system to a first and second memory internal to the computer system when the system is placed in hibernation mode (C 7, L 48-53). This feature provides improved performance by storing the data locally, which reduces delays associated with non-local data transfers. Hence, one of ordinary skill in the art would have been motivated to modify Nicholson's teachings to provide the second memory internal to the computer system for the desirable purpose of improved performance.

Regarding claim 22, Nicholson discloses restoring the state of the CPU when the system is awoken from the hibernation mode (Figure 9, Reference 806).

Regarding claim 23, Nicholson discloses storing the data of the main memory and the state of the CPU to the second non-volatile memory (Figure 7, Reference 714).

Regarding claim 24, Nicholson discloses a driver coupled to the main memory and the first non-volatile memory, wherein the driver writes data of the main memory to the first non-volatile memory (storage driver stack; section [0041], lines 23+; Figure 6, sections [0045] – [0046]).

Regarding claim 25, Nicholson discloses a mobile computer system (section [0028]; a mobile computer system is a computer system used in a mobile environment).

Regarding claims 26-27, Nicholson discloses a hard disk drive (section 0038, lines 17-20); means for storing a state of the computer to a non-volatile memory before power down (Figure 9, Reference 802); means for loading the state of the computer from the non-volatile memory (Figure 9, Reference 802). Nicholson does not explicitly disclose the hard disk drive internal to the computer system. However, Lee teaches the concept of storing the state of the computer system to a first and second memory internal to the computer system when the system is placed in hibernation mode (C 7, L 48-53). This feature provides improved performance by storing the data locally, which reduces delays associated with non-local data transfers. Hence, one of ordinary skill in the art would have been motivated to modify Nicholson's teachings to provide the second memory internal to the computer system for the desirable purpose of improved performance.

Regarding claim 28, Nicholson discloses means for reducing power up time of the computer after being placed in a hibernation mode (section [0023]; when the system loads the data from non-volatile memory cache (Figure 1, Reference 208), the time to power up is reduced since the system does not have to retrieve data from the network).

Regarding claim 29, Nicholson discloses reducing power consumption of the computer (when the system power downs or is placed into hibernation mode).

Regarding claim 31, Nicholson discloses writing the contents to the hard disk drive using a transparent write-through process (data written to the hard disk drive is written in the hard disk drive's cache also and thus the write-through process is transparent to the computer connected to the network, in that the computer writes the data to the remote boot server).

Regarding claim 34, Nicholson does not disclose the second non-volatile memory having the same address configuration as the first non-volatile memory. This concept is well known in the art with cache memory and main memory applications, wherein the cache and main memory having a same address configuration. This feature allows data to written to the cache and the main memory during a write through process, which ensures that the main memory will always be synchronized with the cache in the event of failures. Nicholson discloses the use of the first and second memory to improve reliability in the event of errors or failures and thus it would have been obvious to one of ordinary skill in the art to incorporate this well known concept in the system taught by Nicholson for the desirable purpose of improved reliability.

Regarding claim 35, Nicholson discloses writing the contents of the CPU to the hard disk drive before reducing the power of the hard disk drive (Figure 9, Reference 802);

Response to Arguments

4. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 571-272-4194. The examiner can normally be reached on Mon, Wed, Thurs (10-4), Tues (9:45 - 6:15).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kimberly N. McLean-Mayo
Primary Examiner
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KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

KNM

December 22, 2006